Hall Ticket Number:

Code No. : 17451 N/O

VASAVI COLLEGE OF ENGINEERING *(AUTONOMOUS)*, HYDERABAD

Accredited by NAAC with A++ Grade

B.E. (E.C.E.) VII-Semester Main & Backlog Examinations, Dec.-23/Jan.-24

VLSI Design

Time: **3 hours** Max. Marks: **60**

*Note: Answer all questions from **Part-A** and any **FIVE** from **Part-B***

Part-A (10 × 2 = 20 Marks)

Q. No.	Stem of the question	M	L	CO	PO	PSO
1.	List out the second order effects of MOSFET.	2	1	1	1	1
2.	Define the sheet resistance and area capacitance of a material.	2	1	1	1	1
3.	State the merits and demerits of wet oxidation and dry oxidation.	2	1	2	1	1
4.	Define the Euler path in the stick diagram with an example.	2	1	2	1	1
5.	Compare the merits and demerits of the flip-flop and latch.	2	2	3	1	1
6.	Draw the circuit diagram of 2×1 multiplexer using transmission gates.	2	2	3	2	1
7.	Give significance of sense amplifier in a memory cell.	2	1	4	1	1
8.	Write the importance of floating gate MOSFET in EPROM.	2	1	4	1	1
9.	Write the test vectors to test stuck at faults in two input AND and OR gates.	2	1	5	4,12	1
10.	Define controllability and observability with respect to VLSI testing.	2	1	5	1,12	1
	Part-B (5 × 8 = 40 Marks)					
11. a)	Explain the various forms of nMOS inverter with different loads.	4	2	1	1	1
b)	Design the aspect ratios of pull-up and pull-down transistors in nMOS inverter driven by another nMOS inverter through pass transistors.	4	4	1	3	1
12. a)	Draw the p-well CMOS process flow steps with neat diagrams.	4	3	2	1	1
b)	Discuss the latch-up problem in CMOS technology and list out the remedies.	4	2	2	2	1
13. a)	Design a 8-bit carry skip adder using parallel adders and explain its operation.	4	4	3	4	1
b)	Draw a 4×4 array multiplier and explain its working.	4	3	3	2	1

Contd... 2

14. a)	Design a 4×4 EEPROM memory with an example.	4	4	4	3	1
b)	Design a 4×4 NOR and NAND based ROM architectures	4	4	4	3,12	1
15. a)	Discuss about the testing of IC using level sensitive scan design.	4	2	5	1,12	1
b)	Explain the boundary scan architecture testing method with block diagram.	4	2	5	1,12	1
16. a)	Draw the stick diagram of a Boolean expression, $\overline{A\bar{B}C + DE}$ in CMOS technology.	4	3	2	3	1
b)	Compare the performance of nMOS and CMOS inverter with transfer characteristics.	4	2	1	2	1
17.	Answer any ***two*** of the following:					
a)	Construct a D-flip-flop using transmission gates.	4	3	3	4	1
b)	Compare the working principle of DRAM and SRAM memory cells.	4	2	4	2	1
c)	Discuss the delay fault testing method with an example.	4	2	5	2,12	1

M : Marks; L: Bloom's Taxonomy Level; CO; Course Outcome; PO: Programme Outcome

i)	Blooms Taxonomy Level – 1	20%
ii)	Blooms Taxonomy Level – 2	40%
iii)	Blooms Taxonomy Level – 3 & 4	40%

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